

Figure 2b

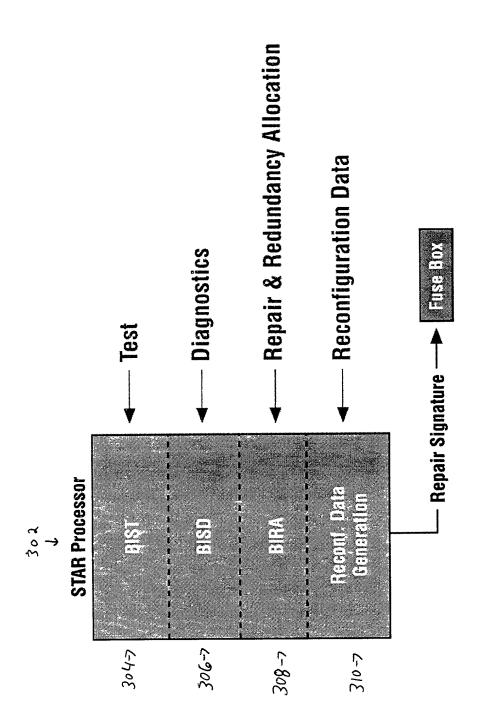


Figure 3

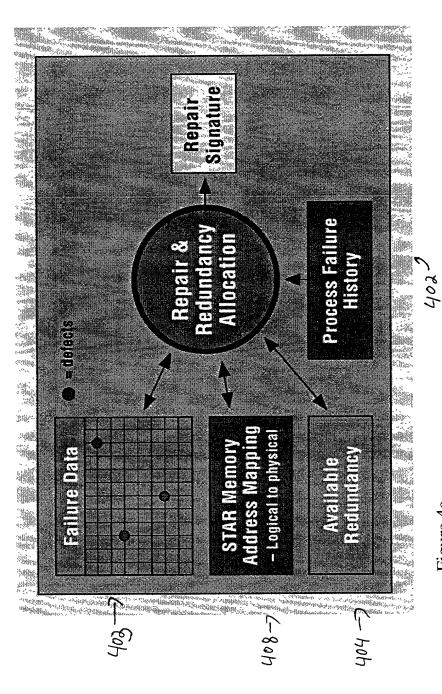


Figure 4a

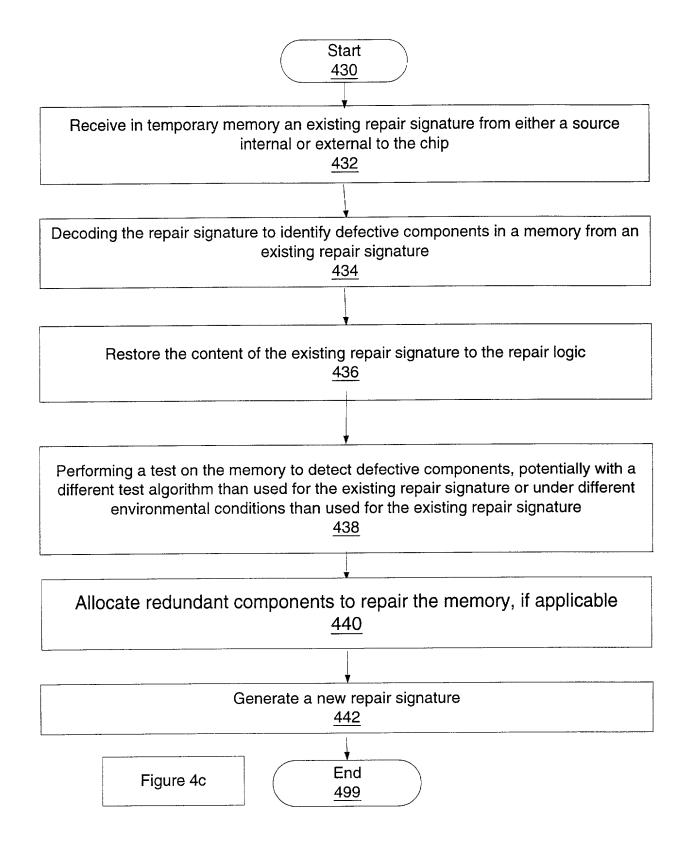
4102 001001000 001001000 0010100101000 01000 0010100101000 **Upper** Lower bank Lower bank Upper bank bank Redundant Status Redundant Redundant Redundant Row column Row **Bits** column 4205 4165 4185 412 5 4145

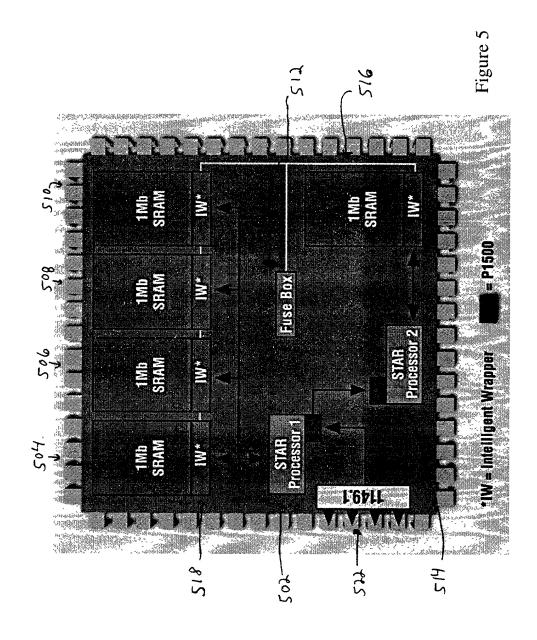
4227

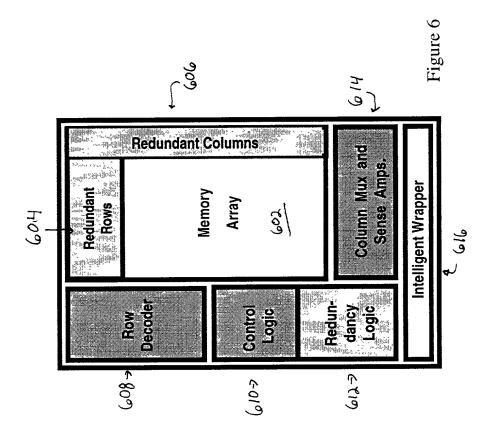
0010100101000	001001000 Upper	01000	001001000 Lower	0010100101000	0100
Upper bank Redundant column	bank	Status Bits	bank Redundant Row	Lower bank Redundant column	Subl/O Status Bits

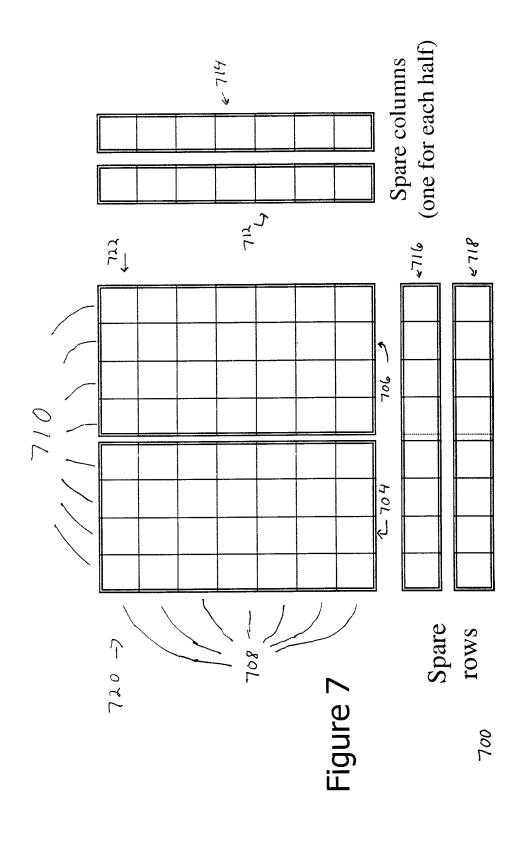
4245

Figure 4b









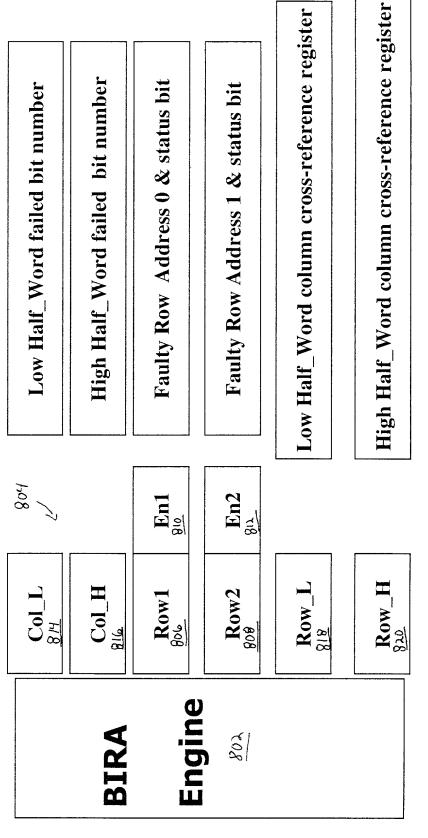


Figure 8

Four Passes Algorithm in Order to Improve Results in the Case of Single Faults in the Row.

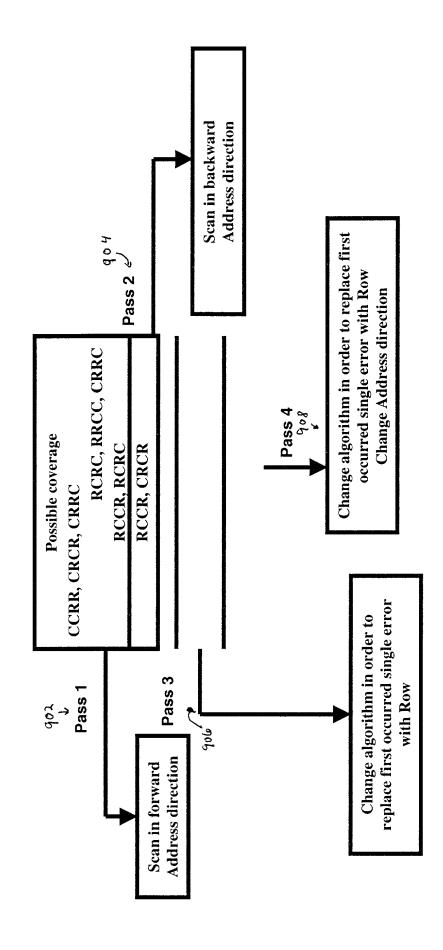


Figure 9

Start condition for BIRA registers

Figure 10

t x01 → 0 1020 Row2 Row\_H H\_IOO En2 X 20401 X ~  $\mathcal{C}$ J 1033 7 4 10347 10382 X 2 X 9 N 8101 1036 ColL ROWI Row\_ C Hhol En1 [0] 10127

Multiple errors in Row fix with Row1 Figure 11

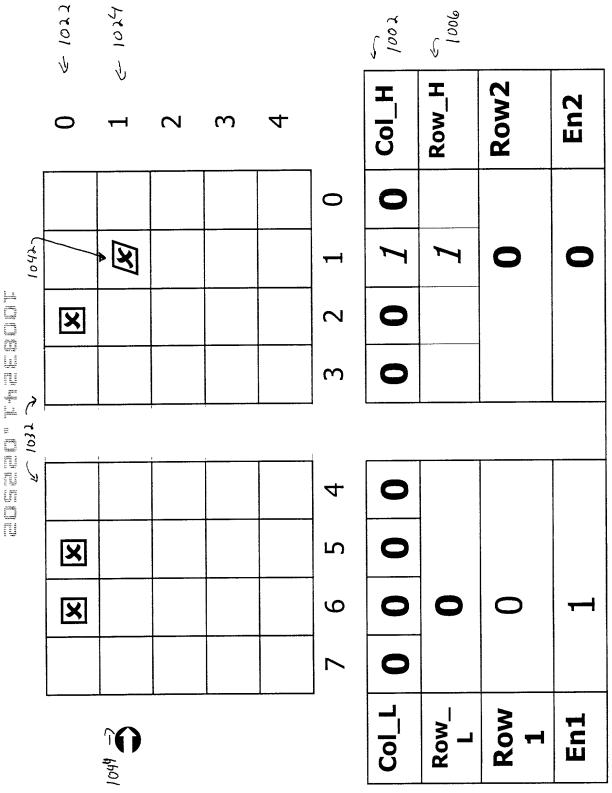


Figure 12 Cover single error with column, register connectivity Row\_H

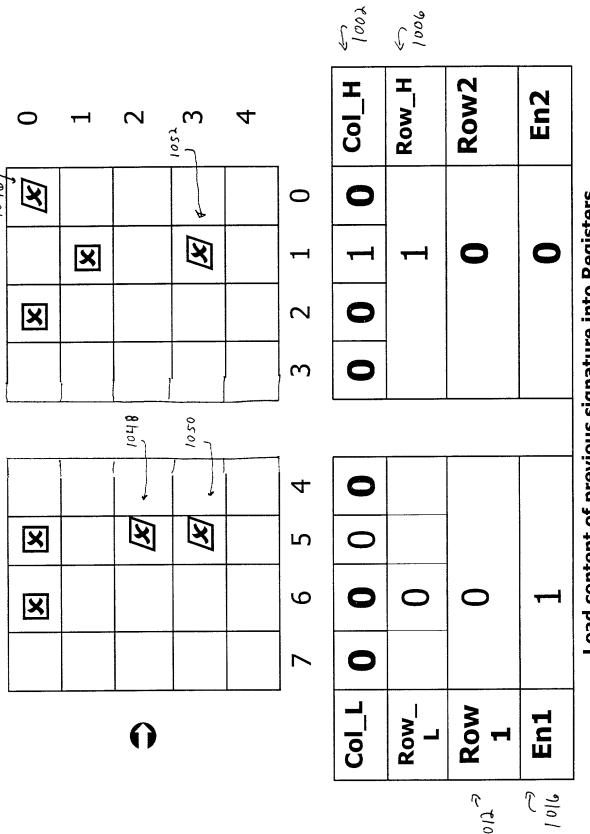


Figure 13 Load content of previous signature into Registers

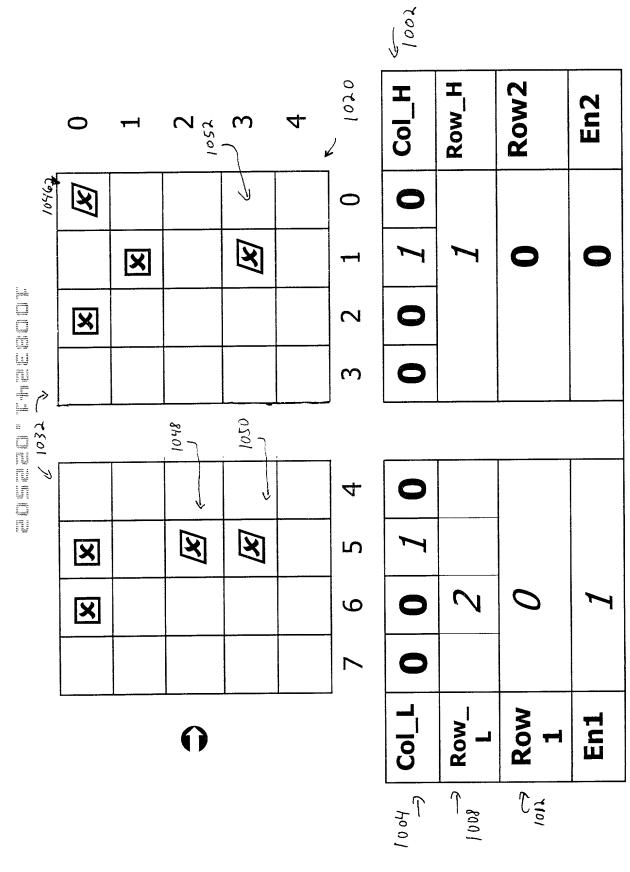


Figure 14 Cover single error with column, register connectivity Row\_L

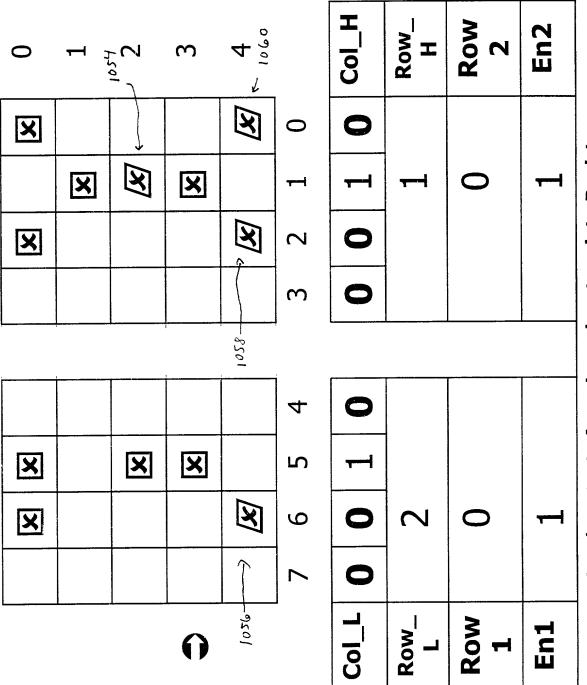
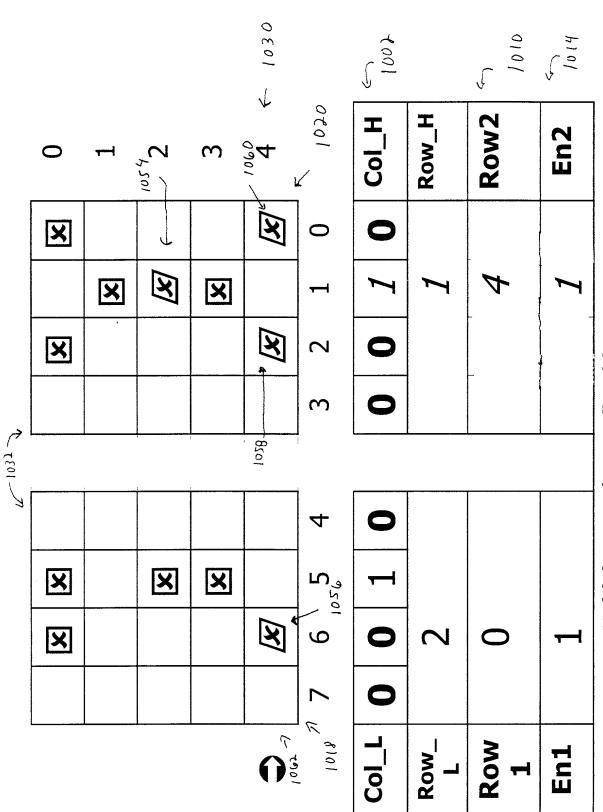


Figure 15 Load content of previous signature into Registers



Multiple errors in Row fix with Row2

Figure 16